

FIG. 1 PRIOR ART

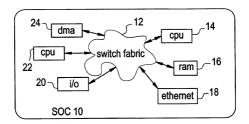
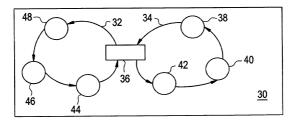


FIG. 2





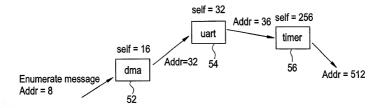


FIG. 4

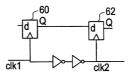


FIG. 5

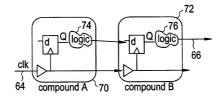




FIG. 6

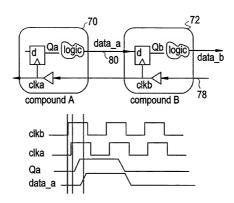


FIG. 7

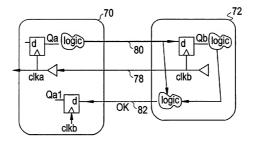




FIG. 8

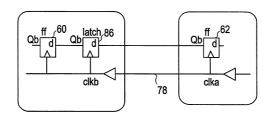
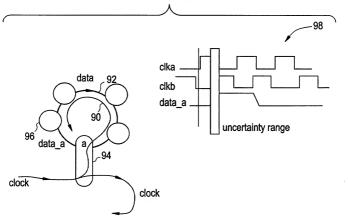


FIG. 9



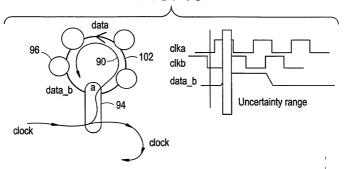
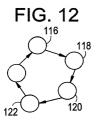


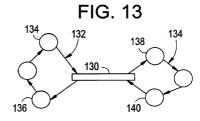
FIG. 11

local_clock 110

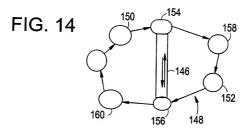
data_in local_data_out 116

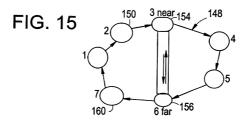
data from previous member clock 112











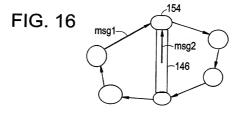




FIG. 17

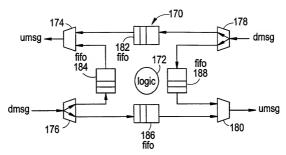
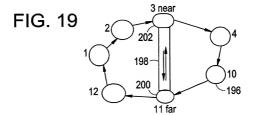


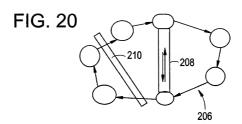
FIG. 18

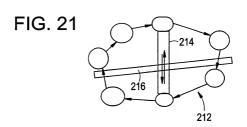
192

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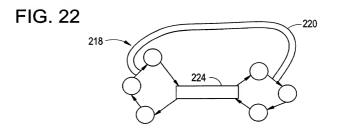
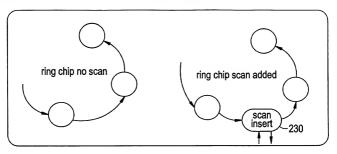




FIG. 23



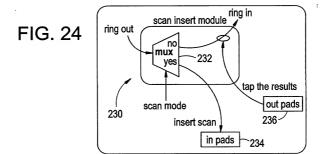


FIG. 25

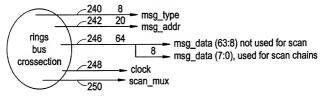






FIG. 26

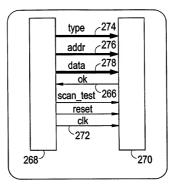


FIG. 27

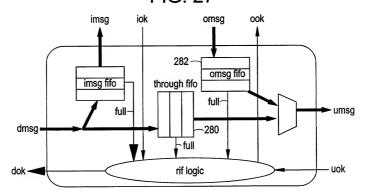




FIG. 29

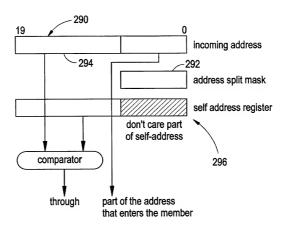




FIG. 30

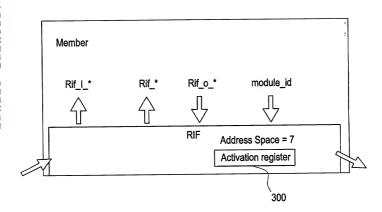




FIG. 31

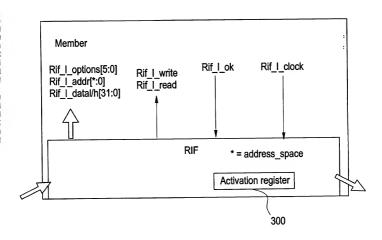






FIG. 32

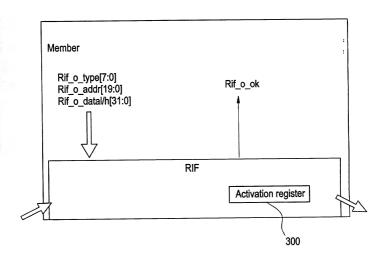
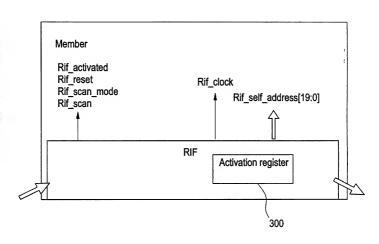




FIG. 33



THE RESIDENCE OF THE PARTY OF T



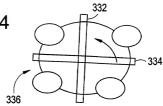
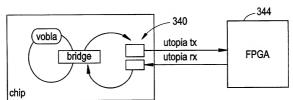
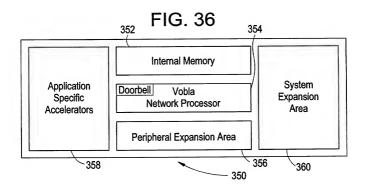
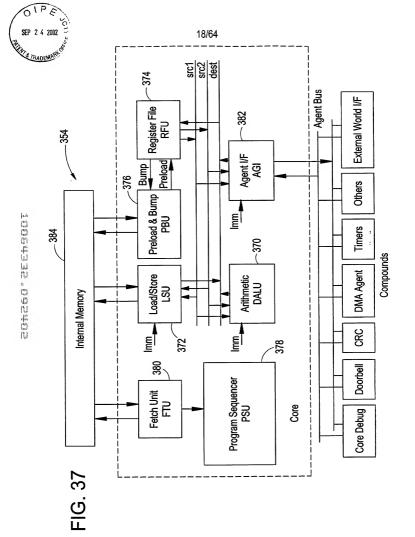
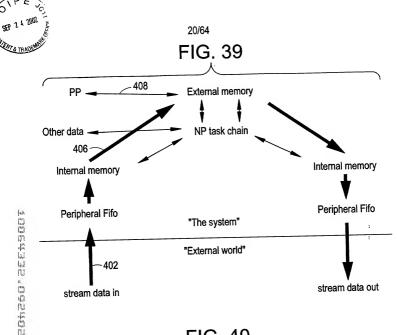


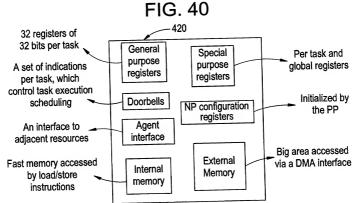
FIG. 35













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FIG. 41

R1 register

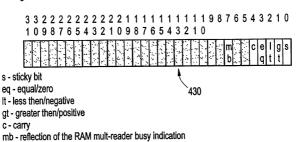


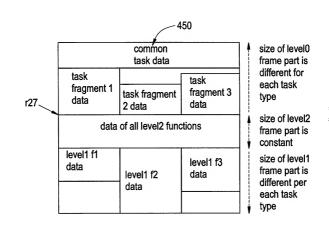
FIG. 42

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1

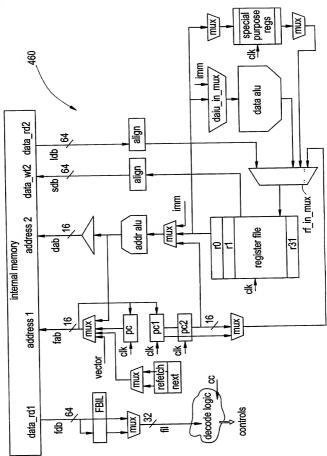
111119876543210

1098765432109876543210 REFETCH SPR REFETCH **NEXT REFETCH** (spr index - 0) 119876543210 65432 3210 CTID NTID TASK SPR 442 (spr index - 1) TRAP SPR A B (spr index - 2) 11119876543210 22222221111 32109876543210 INDEX1 INDEX2 MINDEX SPR (spr index - 3)

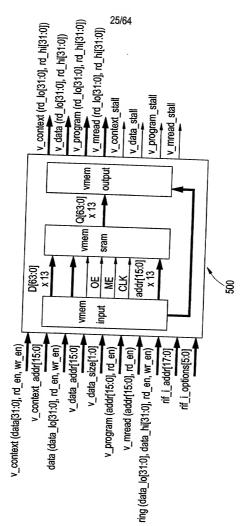






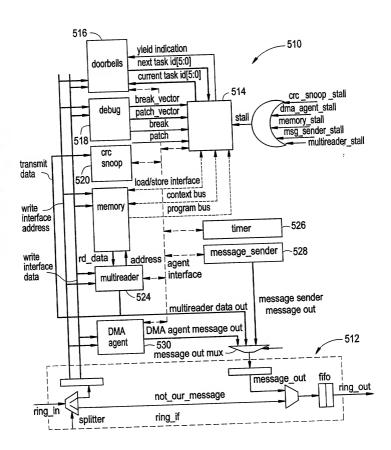




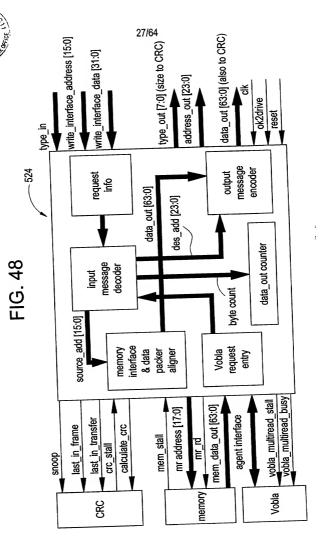








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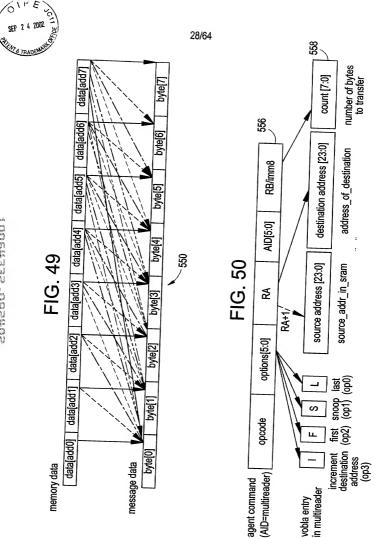
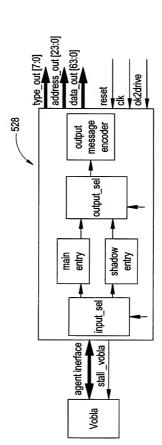
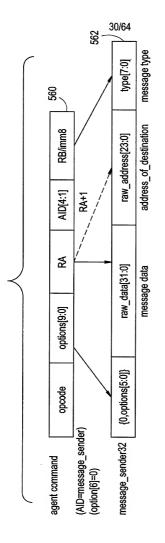


FIG. 51





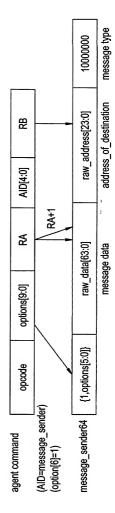
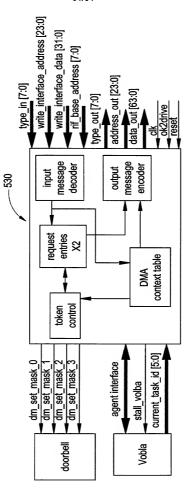
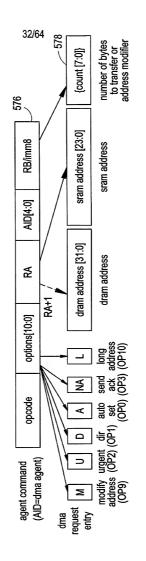


FIG. 53



SEP 2 4 2002 TRADOMENT

FIG. 54



SEP 2 4 2002 SEP 2 TRADEMINE

FIG. 55

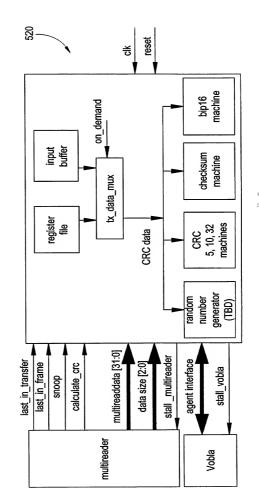


FIG. 56

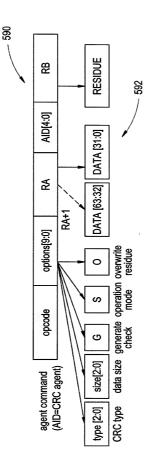




FIG. 57

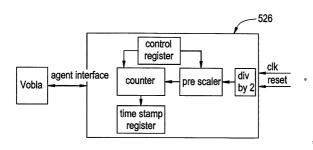
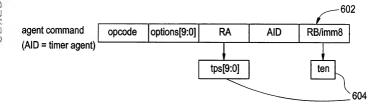
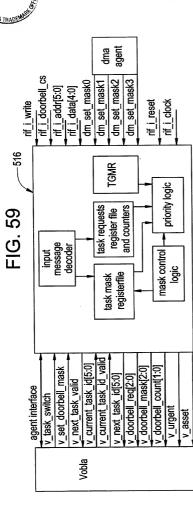


FIG. 58





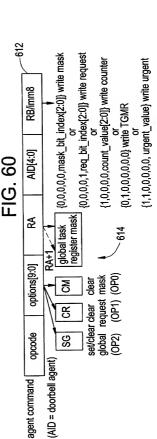
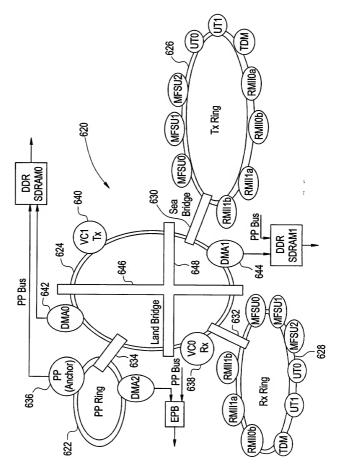


FIG. 61



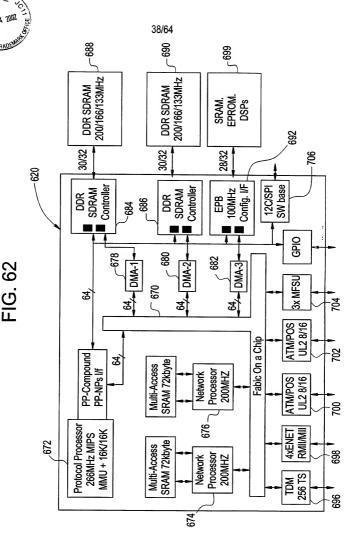




FIG. 63

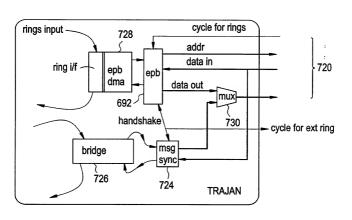
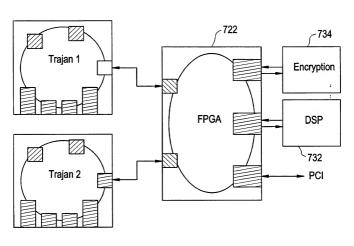




FIG. 64



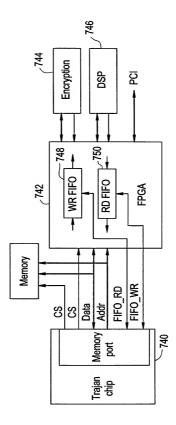
Processor

Functional unit

External ring interface



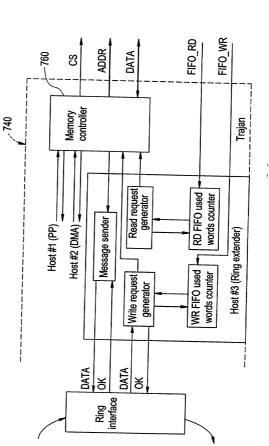
FIG. 65



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FIG. 66





AND ADMINISTRATION OF THE PARTY ADMINISTRATION

FIG. 67

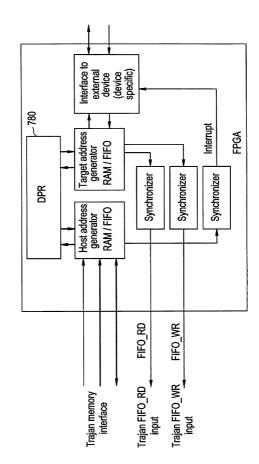




FIG. 68

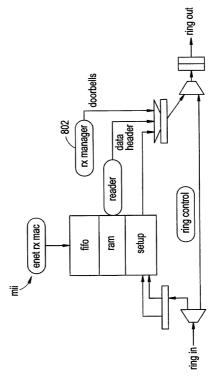
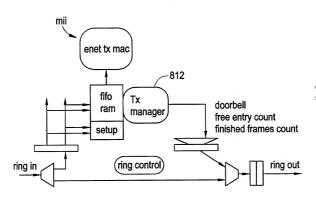
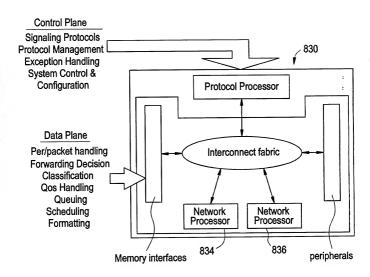


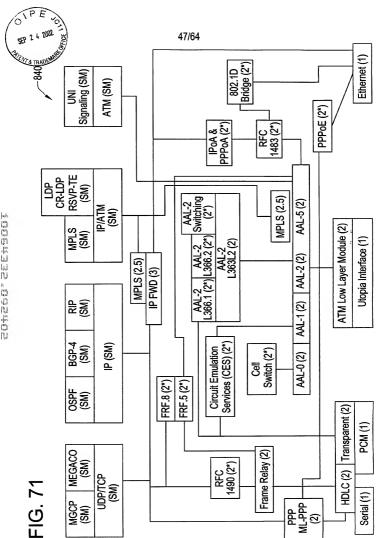


FIG. 69









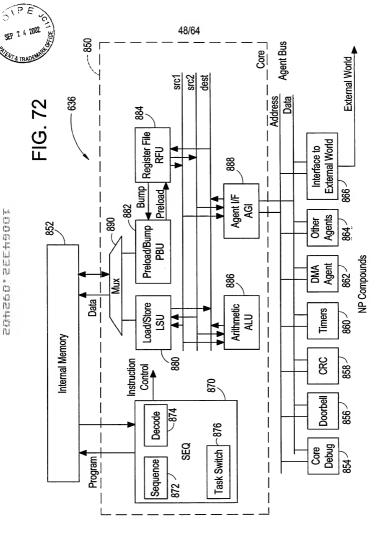




FIG. 74

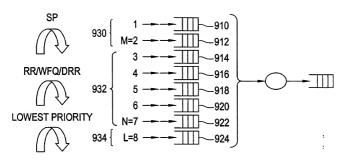
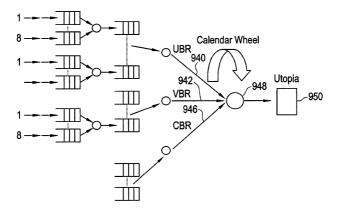
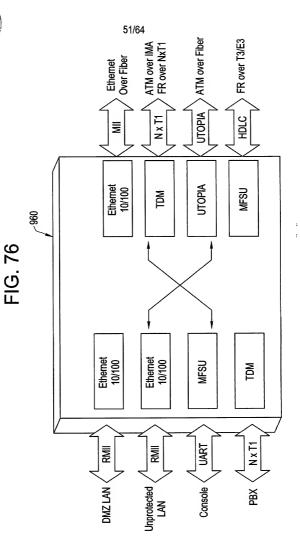
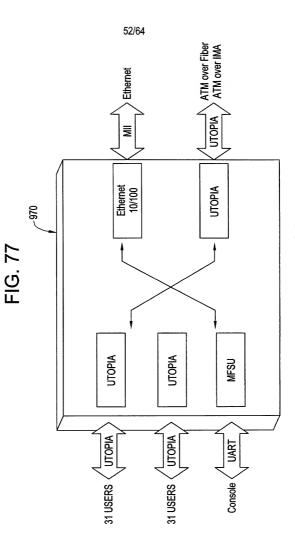


FIG. 75

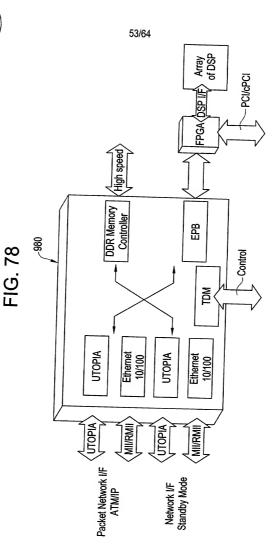


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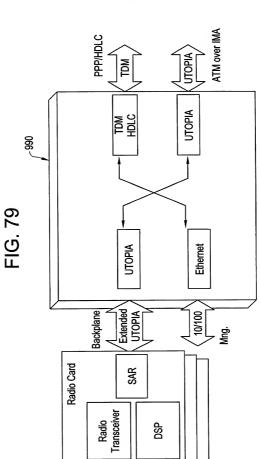




010



OIPE



:

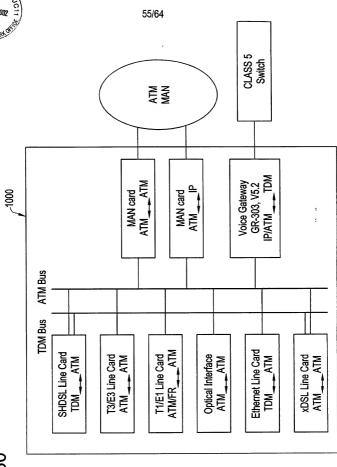
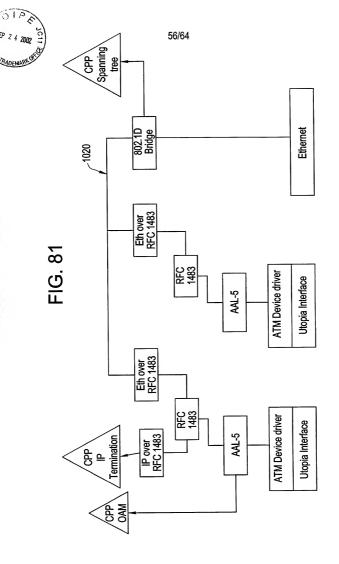
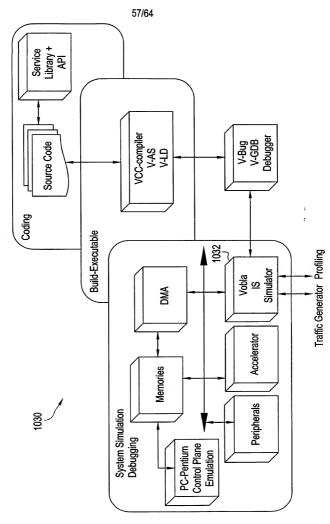


FIG. 80

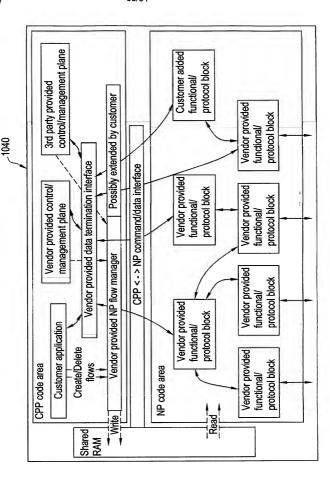


SIPE

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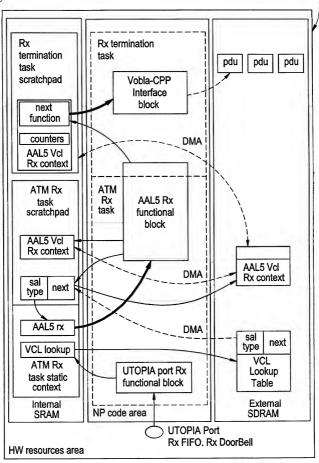


SEP 2 4 2002 11

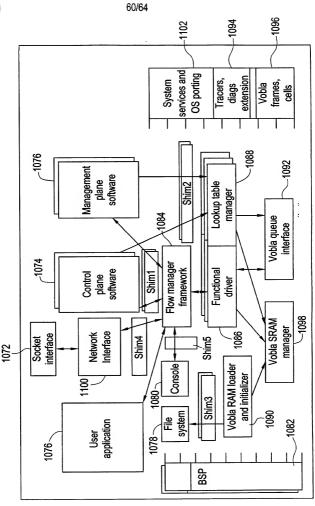
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FIG. 84

1050









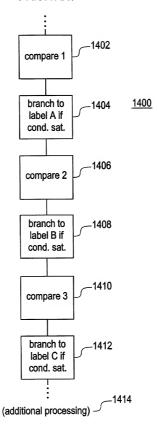
Event logging Computational library Vobla to CPP interface Intertask messaging Frame/cell allocation/release functional blocks Generic system service Fault and exception report . Rx termination processing Congestion control Data queue handling Statistics update Debug support Initialization Generic lookup library Generic frame based shaper Vobla maintenance Generic data path functional blocks processing Bridge Ethernet AAL5, AAL2, AAL1, AAL0 ATM Protocol specific functional blocks data path



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PRIOR ART





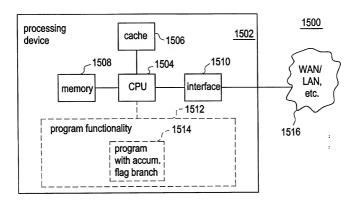


FIG. 89

